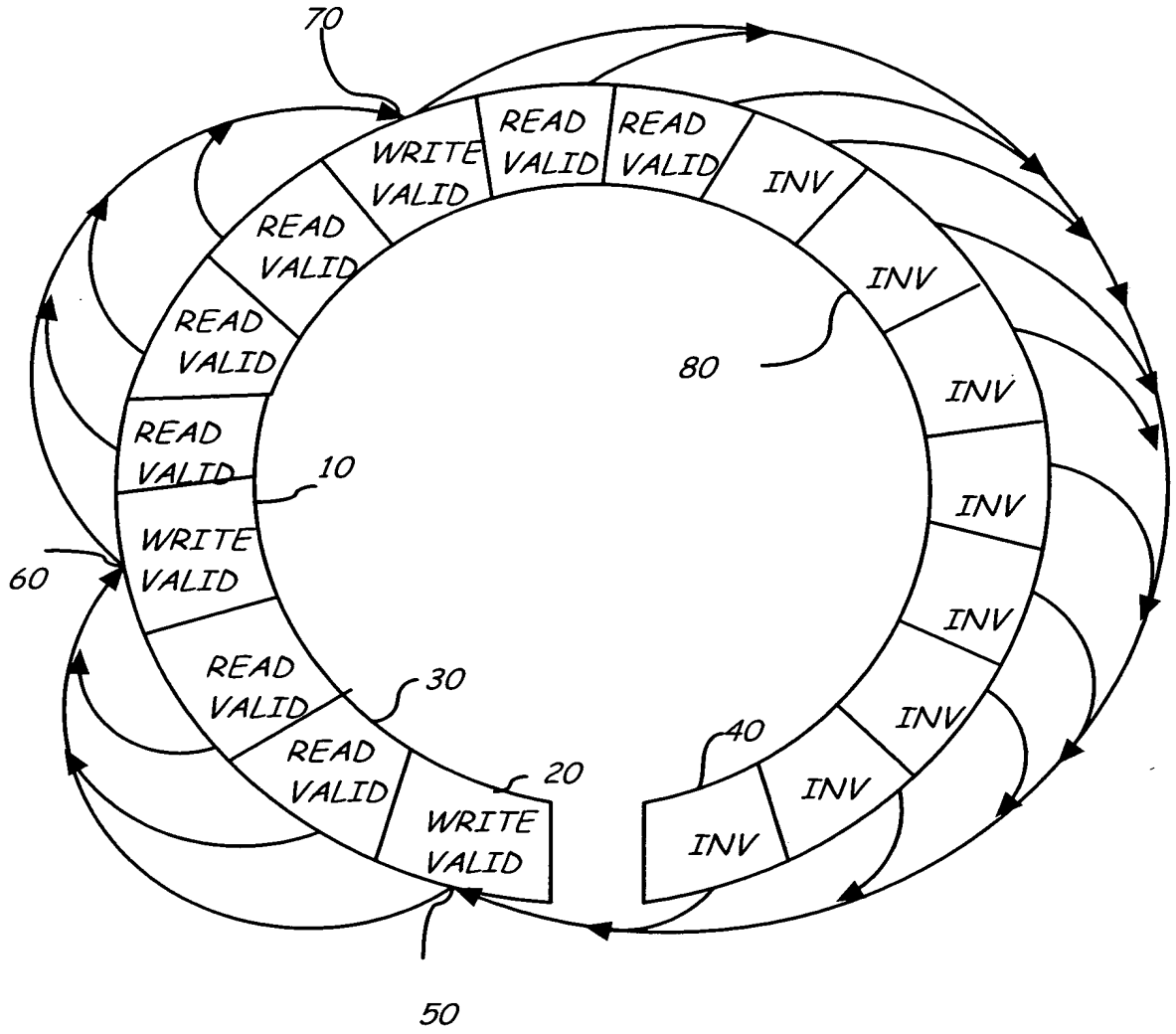
70
WRITE VALID
READ VALID
READ VALID
INV
INV
INV
INV
INV
INV
INV
INV
80
READ VALID
READ VALID
READ VALID
READ VALID
10
WRITE VALID
60
READ VALID
30
READ VALID
WRITE VALID
20
40
50

FIG. 1

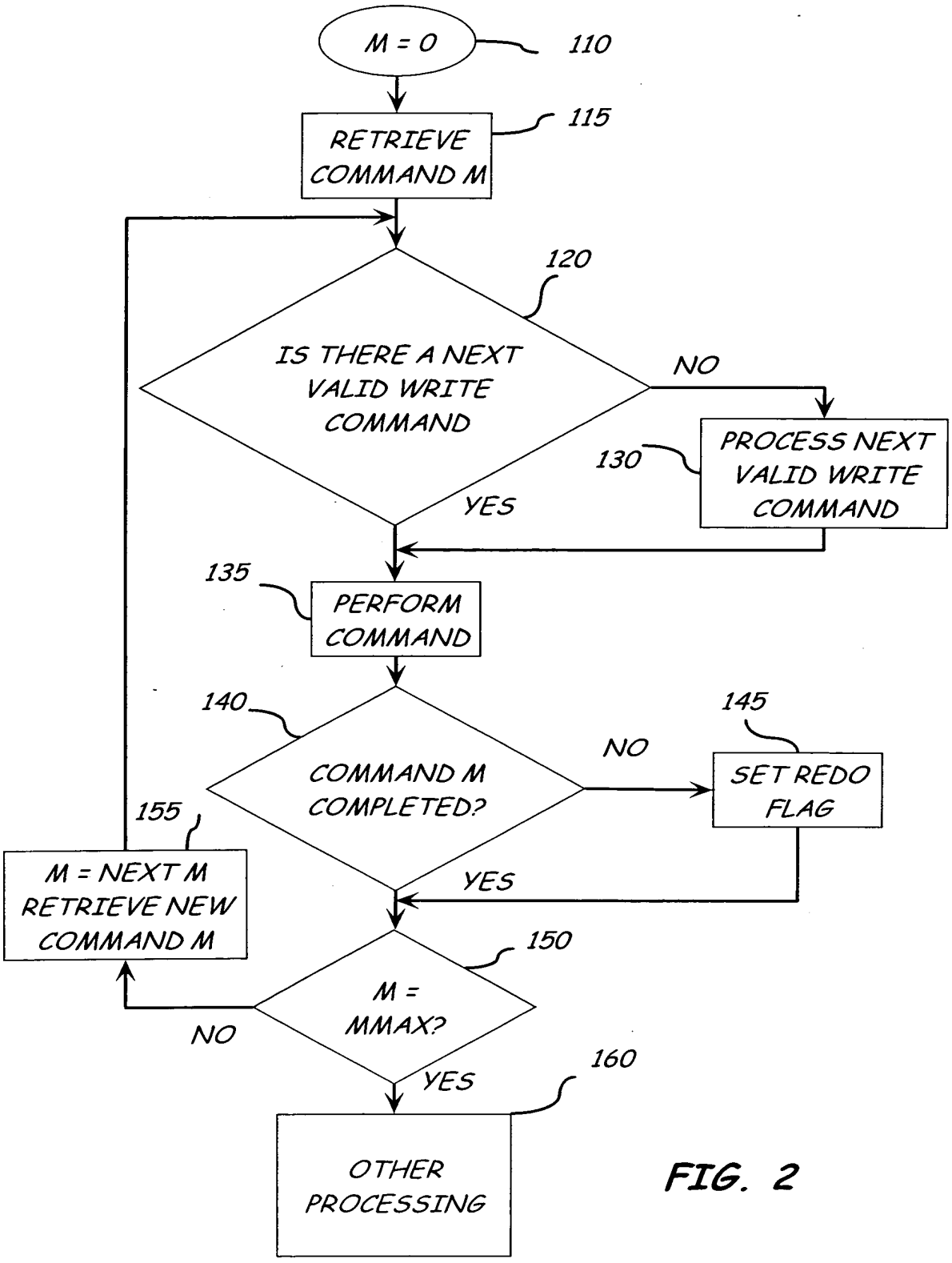
M = 0
110
RETRIEVE COMMAND M
115
120
IS THERE A NEXT VALID WRITE COMMAND
NO
YES
130
PROCESS NEXT VALID WRITE COMMAND
135
PERFORM COMMAND
140
COMMAND M COMPLETED?
NO
145
SET REDO FLAG
YES
155
M = NEXT M RETRIEVE NEW COMMAND M
150
M = MMAX?
NO
YES
160
OTHER PROCESSING

FIG. 2

QUEUE ENTRY	VALID FLAG	DIRECTION	COMMAND	NEXT VALID WRITE ADDR POINTER
0	YES	INBOUND	READ A	6
1	YES	INBOUND	READ B	6
2	YES	INBOUND	READ C	6
3	YES	INBOUND	READ D	6
4	YES	INBOUND	READ E	6
5	YES	INBOUND	READ F	6
6	YES	OUTBOUND	WRITE G	8
7	YES	INBOUND	READ H	8
8	YES	OUTBOUND	WRITE I	6
9	NO	INBOUND	N/A	6
10	NO	INBOUND	N/A	6
11	NO	INBOUND	N/A	6
12	NO	INBOUND	N/A	6
13	NO	OUTBOUND	N/A	6
14	NO	OUTBOUND	N/A	6
15	NO	INBOUND	N/A	6

FIG. 3

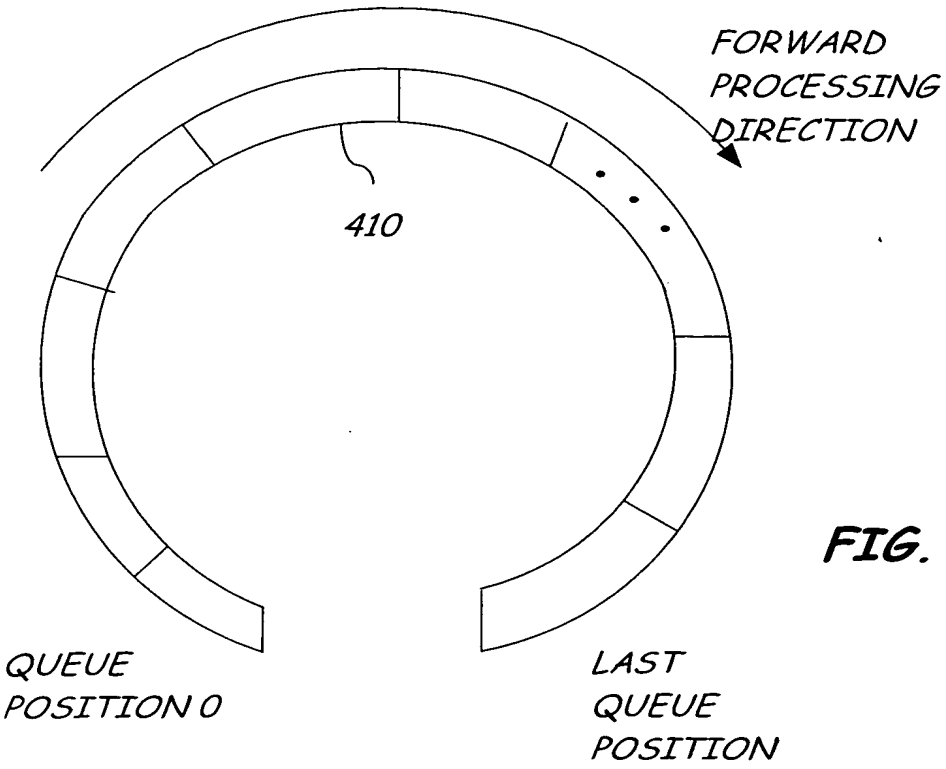
FORWARD
PROCESSING
DIRECTION
410
QUEUE
POSITION 0
LAST
QUEUE
POSITION

FIG. 4

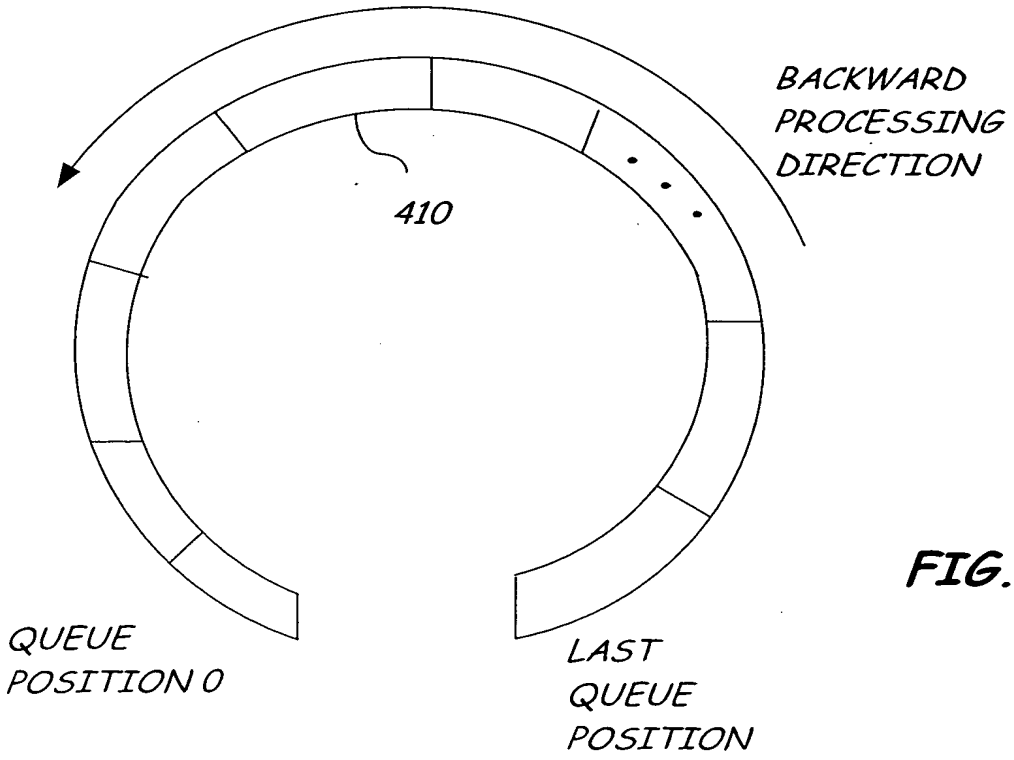
BACKWARD
PROCESSING
DIRECTION
410
QUEUE
POSITION 0
LAST
QUEUE
POSITION

FIG. 5

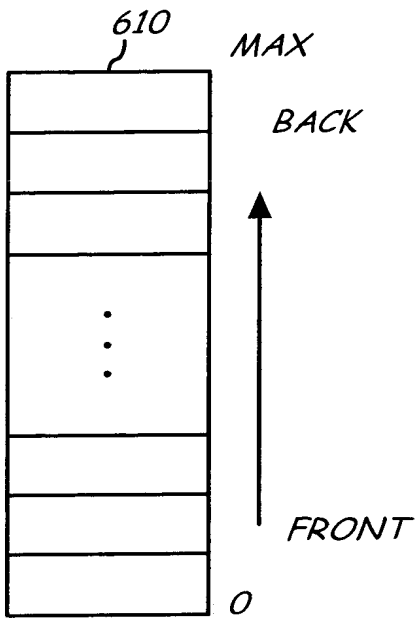

FIG. 6

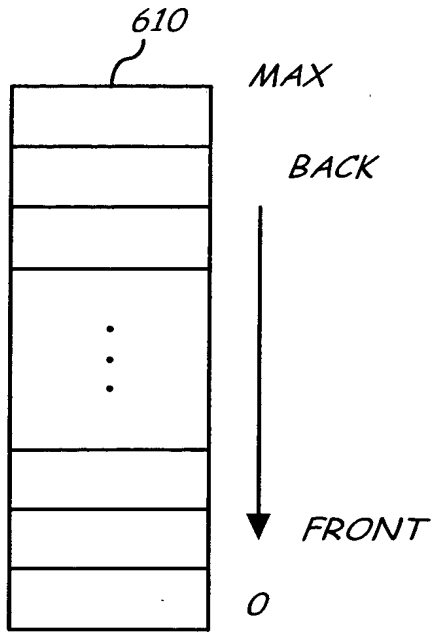

FIG. 7

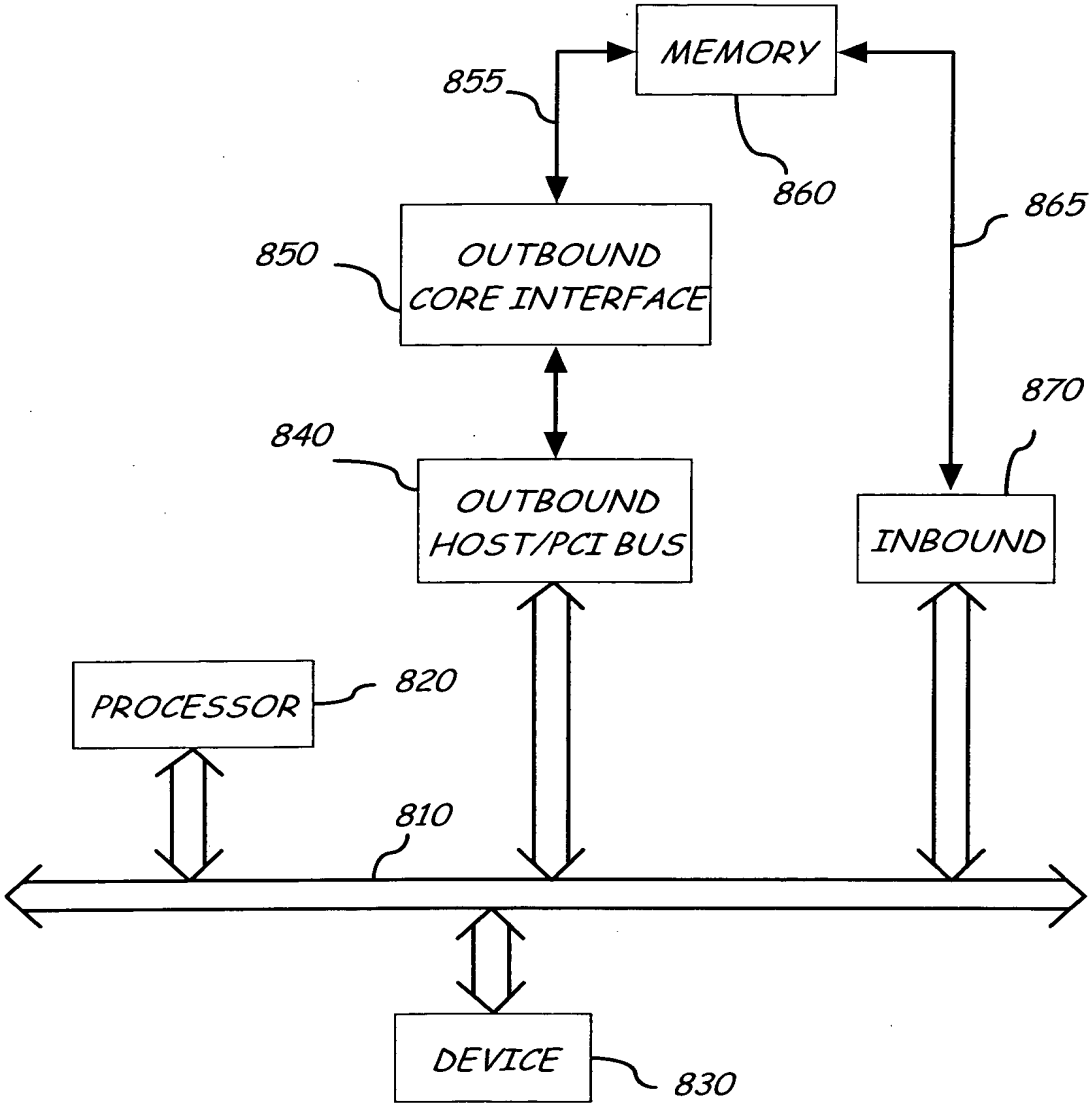
MEMORY
855
860
865
850
OUTBOUND
CORE INTERFACE
870
840
OUTBOUND
HOST/PCI BUS
INBOUND
PROCESSOR
820
810
DEVICE
830

FIG. 8